THAT WHICH IS CLAIMED IS:

1. Process for doping a pattern (3) of electrically isolated resistive elements, characterized in that it comprises steps consisting of:

- electrically and selectively charging the elements (3; 31; 32) of the said pattern;
- adding doping atoms to the said elements as a function of their charge; and
- rebaking the pattern.

2. Doping process according to claim 1, characterized in that the electrical charge is provided by an electron beam or an ion beam.

3. Doping process according to claim 1, characterized in that the electrical charging step of the resistive elements comprises charging the entire pattern and selective discharging of elements by a laser beam.

4. Doping process according to any of claims 1 to 3, characterized in that the step consisting of adding doping atoms consists of adsorbing ions (6; 61; 62) on the surface of the charged elements (3; 31; 32).

5. Doping process according to claim 4, characterised in that the ions are produced by a plasma and are composed of ions derived from atoms chosen from among boron, aluminum, indium, phosphorus, arsenic and antimony.

6. Doping process according to any of claims 1 to 3, characterized in that the step consisting of providing doping atoms consists of implanting ions on the surface of uncharged elements with an energy of less than 100 eV.

7. Doping process according to claim 6, characterized in that the implanted ions are derived from atoms chosen from among boron, aluminum, indium, phosphorus, arsenic and antimony.

8. Doping process according to any of claims 1 to 7, characterized in that elements (3; 31; 32) in the pattern to be doped are made from a semiconducting material.

9. Doping process according to claim 8, characterized in that the elements to be doped are made of silicon, germanium or gallium arsenide.

10. Process for manufacturing an integrated circuit in a silicon substrate (1), characterized in that it comprises the following steps:

- deposition of an isolating layer (2) on the substrate (1);
- deposition of a silicon layer on the isolating layer;
- etching of a pattern of resistive elements (3, 4; 31, 41; 32, 42) in the said silicon layer;

- selective addition of an electric charge on the predetermined elements (3, 31, 32); and
- doping of the elements (3, 31, 32) as a function of their charge.

11. Process according to claim 10, characterized in that the elements (3, 4; 31, 41; 32, 42) of the pattern to be selectively doped are separated by conducting lines connected to a fixed potential during the phase in which electrical charge is selectively added to the pattern.

12. Installation for selective doping of a pattern (3) of electrically isolated resistive elements comprising three chambers (C1, C2, C3) accessible through a single lock (S), characterized in that the first chamber comprises means of selectively charging one or more selected elements in the pattern, the second chamber comprises means of doping elements as a function of their charge, and the third chamber comprises annealing means.

13. Installation according to claim 12, characterized in that:

- the first chamber comprises means of generating an electron beam and focusing it at a precise location of a wafer;
- the second chamber comprises means of generating a plasma of doping ions that can reach a wafer placed nearby; and
- the third chamber comprises means of quickly annealing of a wafer.

14. Installation according to claim 13, characterized in that it comprises a main lock (S) that distributes wafers in the three chambers (C1, C2, C3) through secondary locks (P1, P2, P3).